

In the claims:

Amend claim 1 as follows:

1. (currently amended) A semiconductor device manufacturing method comprising the steps of:

providing a semiconductor substrate having a lower electrically conducting layer thereon and an electrically insulating layer disposed over said electrically conducting layer;

providing a gas etchant comprising a mixed gas of two different fluorocarbon gases, one of said fluorocarbon gases having a low carbon atoms to fluorine atoms ratio (hereinafter C/F ratio) and the other of said gases having a high C/F ratio, the fluorocarbon gas having the higher ratio of carbon atoms to fluorine atoms forming more than ~~at least~~ one half of the mixed gas; and

etching a connection hole through said electrically insulating layer in a single etching step to said electrically conducting layer using only said mixed gas as the etchant.

2. (canceled)

3. (currently amended) A semiconductor device manufacturing method as described in Claim 1 wherein C_4F_8 is used as the fluorocarbon gas having a higher ~~lower~~ ratio of carbon atoms to fluorine atoms and at least one selected from the group composed of CHF_3 , CH_2F_2 , and CF_4 is used as the fluorocarbon gas having a lower ~~higher~~ ratio of carbon atoms to fluorine atoms.

4. (previously presented) A semiconductor device manufacturing method described in Claim 1 wherein the insulating layer is plasma-etched with the mixed gas of fluorocarbon gases.

5. (previously presented) A semiconductor device manufacturing method described in Claim 1 further including an upper electrically conducting layer connected to the lower electrically conducting layer formed in the connection hole as an electrode or wiring.

6. (previously presented) A semiconductor device manufacturing method described in Claim 5 wherein the lower electrically conducting layer has a titanium nitride layer on the surface where the connection hole is formed and the electrically insulating layer includes a spin-on glass layer.

7. (previously presented) A semiconductor device manufacturing method described in Claim 6 wherein the lower electrically conducting layer is made of a stacked structure having a titanium nitride layer, a layer of aluminum or an alloy thereof, a titanium layer, and a titanium nitride layer stacked in that order, and the electrically insulating is made of a stacked structure having a silicon oxide layer formed from tetraethylorthosilicate, a spin-on glass layer, and a silicon oxide layer formed from tetraethylorthosilicate stacked in that order.

8-9. (canceled)